Detection and Impact of Cracks Hidden Near Interconnect Wires in Silicon Solar Cells

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***Abstract* — The thermal stresses associated with the soldering of interconnect wires onto the busbars of solar cells is one of the leading causes of cracks in silicon solar cells. Cracks will often branch outward from the busbar region so that they are easily seen in an electroluminescence (EL) image. However, since the wires are often wider than the busbar metallization, cracks can be located underneath or close to the wires and be "hidden" within the EL image. If the cracks remain beneath the busbar metallization, they may cause no reliability problems. However, if they propagate along the side of busbars and remain hidden under or next to the wires, they can prevent continuity of the gridlines to the busbars. The cracks may cause minimal problems in a new solar panel, but over time they can open up with thermal cycling and cyclic loading in the field. We demonstrate how these hidden cracks may be detected with the technique of UV Fluorescence, and we show examples of their signature in EL images. It is our observation that many groups are not familiar with these EL signatures, and do not consider that hidden cracks may be the cause of many gridline interruptions. We also show how gridline corrosion is strongly linked to hidden cracks where moisture can penetrate through the cracks. We hope that these techniques and improved understanding can lead to improved testing and feedback that accelerate product development and improve panel reliability.**

I. Introduction

Electroluminescence (EL) is the main technique used to image defects in silicon solar cells. EL is now commonly performed in solar panel factories at the following stages for every solar panel: 1) After interconnecting the cells with soldered wires, today commonly forming a 10 or 12-cell string of rectangular cells; 2) At the layup table after placing strings of cells on glass/encapsulant and interconnecting the strings with bussing wire; 3) After lamination prior to packaging. Commonly seen defects are 1) Long cracks that commonly start and end at either a cell edge or a wire location, 2) short "V-cracks" most commonly at the tips of wires or where wires cross a cell edge, 3) short "X-cracks" due to sharp impacts, 4) dark bands along a portion of the wire due to cold solder joints between the wires and silver busbars, 4) dark bands along an entire wire due to a cold solder joint between the bussing wire and the interconnect wire, 5) dark gradient bands along a silver gridline due to a break in the gridline from a screen printing defect where the band is darkest near the break and lightest near the wires, and 6) dark bands along a silver gridline where the band is darkest next to a wire. The origin of this last defect is commonly attributed to a break in the gridline metallization near the wire, but the understanding of how these breaks occur and the risks they pose is not commonly understood. Kang [1] referred to these as *DR* (Dark Rectangular) defects and showed how they became more severe with an increasing number of thermal shock cycles, and hypothesized about how the damage may be linked to changes in the microstructure of the solder, despite showing an image where the break in a gridline clearly was located over a crack in the silicon. Earlier, Lin [2] referred to these as *GFIB* (GridFinger Interruption at Busbar) defects, and found them to be the main contributor to P_{max} degradation in Humidity Freeze testing, but did not speculate on the details of how the interruptions occurred. Earlier still, Chaturvedi [3] studied the dark rectangular defects and accredited them to stresses between the soldered wires and gridlines that caused cracks in the gridlines, but not the underlying silicon. The oldest publication from Q-Cells [4] suggested the term *GICS* (Gridlines Interrupted Caused by Soldering) and correlated some of these interruptions to microchips in the silicon. A microchip is a scallop shaped crack that is largely parallel to the face of the cell and which does not extend through the thickness of the cell but which can intersect the top cell surface along a line. Where this line intersects the gridlines, cracks in the gridlines can occur. We find the Q-Cells analysis the most convincing of the literature we surveyed.

In this paper we aim to reintroduce and expand upon the *GICS* defect concept and explain further how different types of cracks hidden under or near the interconnect wire can leads to defects seen within EL images. We revisit older environmental chamber data and temperature-effect data that can lead to crack opening/closing, and we show new UV Fluorescence data that clearly shows the location of cracks through the thickness of the silicon that are hidden beneath or adjacent to the interconnect wires.

II. Model for Gridline-Busbar Discontinuity

Figure 1 shows an example of monocrystalline cells within a panel with polymer backsheet that we placed under static and cyclic mechanical loading stresses. These EL images and subsequent images from our groups were captured with a BrightSpot Automation EL camera system with 24 Megapixel resolution and with the panel biased at $-I_{sc}$. The cells show a variety of cracks across which the metallization is discontinuous to varying degrees. The red outlined regions show examples of *GICS* defects that may be due to hidden

cracks adjacent to a) the left busbar, and b) to both the left and right busbars.

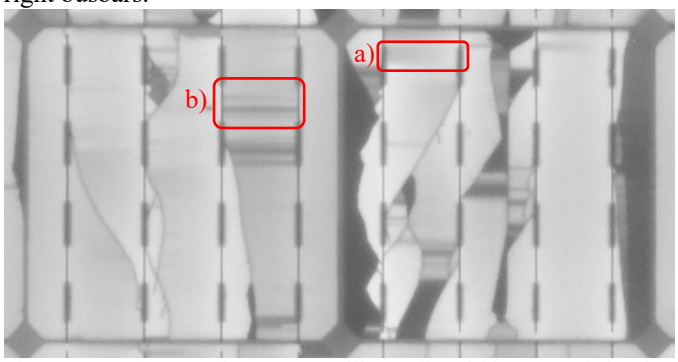

Fig. 1. EL image of monocrystalline cells within a panel that has undergone mechanical load testing and which shows various types of cracks. The red circled regions show examples of GICS defects that may be due hidden cracks adjacent to a) the left busbar, and b) to both the left and right busbars

The drawings in Figure 2 show how a crack adjacent to a busbar could be hidden from EL imaging by the interconnect wire. Such long cracks may be propagated from sub-millimeter microcracks originating from the differential contraction between the copper wire and the silicon during cooling during the soldering process [5]. The crack may wander, sometimes also falling under the busbar or even slightly beyond the wire and still be obscured from EL imaging. Cracks may propagate through the entire thickness of the silicon, or they may be roughly parallel to the surface as in the Q-Cells microchip example [4].

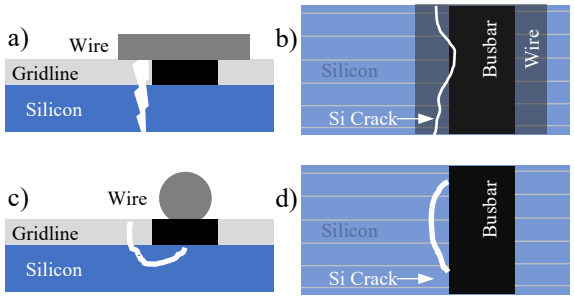

Fig. 2. Drawings of the cross section and top view of solar cells with cracks near the busbar. In a) and b) a flat ribbon wire and a crack running through the thickness of the cell are shown, while in c) and d) a round wire and a microchip crack running roughly parallel to the cell are shown.

If the entire interface between the busbar and the wire is well soldered, then a crack under the busbar location should not cause a gridline discontinuity since the current can enter the wire before being blocked by an open crack. However, the solder might only be bonded well to discrete "solder pad" locations along the busbar, leaving some percentage of the busbar sensitive to cracks under the busbar, leading to GICS defects. It is unclear how well the solder may bond directly to the silver gridlines, and this likely varies significantly among manufacturers, but well bonded gridlines would provide good resistance to GICS defects for cracks that propagate along the wire/gridline interface region. In modern panels with wire array interconnects using 9 or more round wires, there may be little wire/gridline interface region where cracks could be completely hidden, but cracks just alongside the busbars may still be obscured from EL imagery. In addition, the busbars on the rear side of the cells often have wider bonding pad regions as can be seen in Figure 1. The higher surface recombination in these regions cause the EL image to be darker above the bonding pads, making it more challenging to see cracks in those regions.

Our older publication [5] shows some evidence for the microchip variation of *GICS*. Figure 3 shows how a wire pull test can pull up chunks of silicon with relatively little force on badly soldered cells, presumably due to the existence of crack planes in the silicon that do not penetrate through the entire thickness of the wafer. Figure 3 also shows an SEM cross-section image where a crack roughly parallel to the cell surface can be seen.

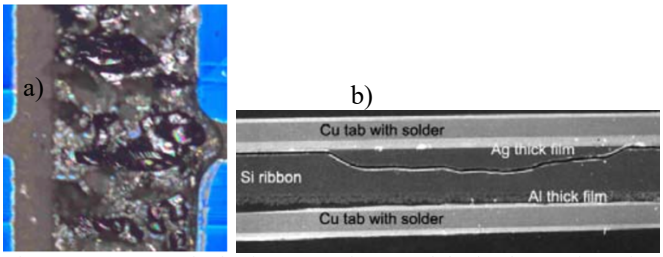

Fig. 3. a) An optical microscope image of the busbar region after a wire has been pulled off, taking chunks of silicon with it, and b) an SEM cross section of a soldered cell showing a scallop crack roughly parallel to the surface of the cell. Both images taken from [5].

III. Temperature Effects on Gridline Discontinuity

Figure 4 shows the crack closure and improvement in metallization continuity that occurs when heating a panel by applying a forward bias current [6]. Silverman has also seen changes in the continuity of metallization by heating and cooling effects and has measured the change in the width of gap across the cracks with changes in temperature [7]. It is not clear how the change in the state of *GICS* defects could be explained in the absence of cracks.

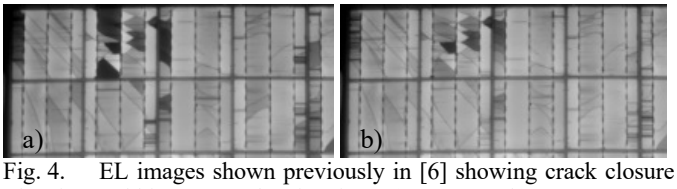

Fig. 4. EL images shown previously in [6] showing crack closure after forward bias current heating from a) 20.6 C to b) 35.3 C. Some *GICS* defects improve significantly.

IV. Mechanical Loading Effects on Gridline Discontinuity

We have published previously on the concept of crack opening with front side mechanical loading and crack closure with rear side loading [8,9]. Figure 5 shows EL images of a panel with many cracks and *GICS* defects that we previously had placed under rear side load with a *RailPad* brace to place the cells into compressive stress and close previously open cracks. Again, it is not clear how the change in the state of *GICS* defects could be explained in the absence of cracks.

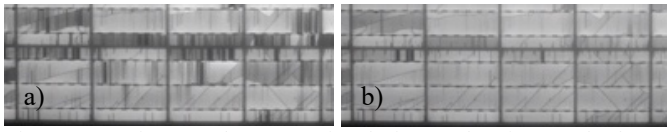

Fig. 5. EL images shown previously in [8] showing crack closure after rear side loading with a *RailPad* brace. Most *GICS* defects improve significantly.

V. Machine Learning Detection of Gridline Discontinuities

We have developed and trained a machine learning model to automatically detect a range of different defects related to cracks and soldering/wire problems. The *GICS* defect can often present itself as a narrow dark line that might be confused by the model as a short "non-branching crack" defect. However, these defects are always perpendicular to the busbars and thus show little confusion with other defect types, and our model handles these inferences well as can be seen below in Figure 6. The challenge for automating the detection of the *GICS* defect is related to the wide variability in darkness contrast with the surrounding region. If one annotates every minor occurrence of the *GICS* defect in the training data, then the operator may be overwhelmed with inference detection events in cases where this defect type is common.

Fig. 6. Successful machine learning inference of a GICS defect signature.

VI. UV Fluorescence of Panels with Cracks Near Busbars

UV Fluorescence (UVF) is a panel characterization technique that can be used to image a wide variety of defects in field aged or environmental-chamber aged panels [10,11]. In panels with polymer backsheets, it is particularly powerful at imaging cell cracks since oxygen can diffuse through the polymer backsheet and through the cracks and spread laterally a few mm's to quench the fluorescence in the front encapsulant such that a wide dark line is easily seen around the crack locations. Since the dark lines are much wider than the wires, cracks near or under the wire locations that would normally be hidden in an EL image are easily seen in the UVF image. In this work, we captured UVF images of fielded panels with a BrightSpot Automation pole mounted UVF camera system with a UV flash.

Figure 7 shows UVF images of fielded modules that indicate extensive cell cracking near the busbar locations on most cells. In some cases, the cracks appear to be very short, resulting in more of a dot shape than a line, while in many cases, the crack or series of shorts cracks cause the entire busbar region to be dark. While most cracks remain confined to the busbar regions, some cracks have propagated at an angle into the region between busbars. In the SolarWorld panel, narrow dark lines parallel to gridlines emanate from the busbars which we attribute to gridline corrosion. It is significant that the corrosion only spreads from busbars with cracks, indicating that the hidden cracks play an important role in the corrosion. We hypothesize that moisture can penetrate the cracks and react with the front encapsulant to form acetic acid that attacks the silver metallization and gradually works its way down the length of the gridlines. Such corrosion can result in high contact resistance between the silver and the silicon [12] and reduced line resistance along the length of the gridlines.

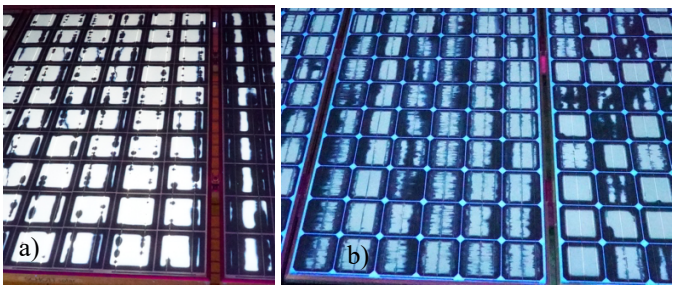

Fig. 7. UV Fluorescence images of panels with extensive cell cracking near busbars: a) Schott Solar after 11 years in CO; b) SolarWorld after 10 years in MA where gridline corrosion is seen.

While the classic UVF image exhibits dark lines over the crack regions, some panel designs exhibit a white line over the crack regions. This presumably is related to rear encapsulants with a high concentration of fluorophores that can diffuse through the cracks to the top encapsulant layer. The competing kinetics of oxygen diffusion through the crack to quench the fluorescence is apparently insufficient to overpower the strong diffusion of the fluorophores in these cases. The UVF image shown in Figure 8 shows interesting variations in the brightness of 3 cracks. The left crack along the edge of the isolated area fluoresces white in a narrow band, while a wider dark band from the oxygen quenching behavior is seen where the crack crosses the strongly fluorescing ring. This bright ring is due to fluorophore diffusion from the gap region between cells. The middle crack only shows the dark band. It is unclear why different cracks have such different behavior, but it is perhaps

related to the width of the gap in the silicon across the crack. The right crack is very close to the wire and leads to strongly fluorescing wire regions, presumably due to the diffusion of the fluorophores over the wire and to the higher reflectivity of the wires. Smaller regions where the left crack is near the wire also show this behavior. Thus, we can conclude that strongly fluorescing wires also are an indicator of cracks near to or underneath the wires.

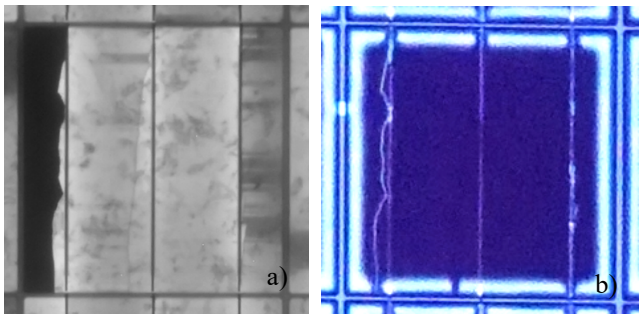

Fig. 8. a) EL image of a cell from a Jinko JKM305P-72 panel showing 3 cracks; b) the corresponding UV Fluorescence image where the left crack fluoresces white, the middle crack is easily seen only where it causes a quenching of the fluorescence in the ring region, and the right crack causes white fluorescence above the wire.

VII. Discussion

The temperature effect and mechanical loading data suggest that many of the *GICS* defects are due to cracks in the silicon. It seems more likely that these observed cracks are of the type that penetrate the full thickness of the wafer rather than the microchip variety. More characterization is needed to show the relative prevalence of cracks in *GICS* defects and to demonstrate whether there are cases where such defects are present without cracks in the silicon. By studying the prevalence of such defects in panels from different manufacturers, we can better understand the design and process factors that make panels resilient to these defects.

Based on the UVF data, we see that there are cases where most busbar regions have cracks in the silicon that have propagated through the thickness of the wafer, even if the cracks rarely propagate into the region between busbars where they can be imaged by EL. Indeed, these may be the most common type of crack in the silicon PV industry. The degradation risks are that 1) these cracks open up over time, leading to visible *GICS* defects in the EL images, 2) that these cracks propagate away from the busbars under mechanical load or thermal cycling, leading to isolated regions, and 3) that they enable gridline corrosion.

Panel manufacturers have internal quality control guidelines based on EL testing at various stages, where a detected crack may prompt rework prior to lamination, or where a certain frequency of cracks in the panel post-lamination results in a downgrade in the class and selling price of a panel. The fact that we may be missing a large percentage of cracks by EL imaging raises concerns for panel reliability. Additionally, a misinterpretation of the dark finger bands seen in EL images can mean that manufacturers are not accurately following their own internal quality metrics. For example, a GICS defect that occurs between a busbar and the edge of the cell or when gridlines are not connected to any busbar due to GICS defect at each neighboring busbar, the dark region in the EL image is close in nature to an "isolated area," and the grading score for a crack defect would be very different than that of a screen printing defect. For panel grading criteria such as the MBJ Solar Module Judgment Criteria [13], commonly used in field EL testing, the grader is tasked to assume that any crack will continue to propagate in the direction it is heading, and the implications of the *GICS* defects being due to cracks could have a severe impact on panel grading scores.

During product development, panels normally undergo extensive environmental chamber testing. Thermal and/or UV exposure can cause the evolution of fluorescence in the front encapsulant when illuminated by UV light. This raises the possibility of using UVF during product development to help detect the hidden cracks, at least for panels with polymer backsheets. Many modern panels use a front encapsulant without UV absorbing additives, and such panels exhibit "ring pattern" fluorescence where it is more challenging to see cracks over the whole cell area. By using front encapsulant with UV absorbing additives for special product development work, the hidden cracks may be more easily detected by UVF.

VIII. Conclusions

Cracks within the silicon wafer near the busbar regions are common within the PV industry, and these cracks are often obscured from detection by EL imaging. We suggest reimplementing the old *GICS* defect (Gridlines Interrupted Caused by Soldering) terminology proposed by Q-Cells [4] to refer to the dark bands in EL images parallel to the gridlines. The silicon cracks can be of the *microchip* variety and can cause breaks in the gridlines where the cracks intersect the gridlines. The cracks can alternatively propagate through the entire thickness of the silicon, and we present UV Fluorescence (UVF) data that confirms the widespread presence of such cracks. These dark rectangular EL defects are presently not well understood within the PV community, and definitively assigning them to a subcategory of crack defect has potentially significant financial implications in terms of how panels are graded for quality, factory yield, and insurance/warranty claims.

We demonstrate how gridline corrosion appears to be well correlated to the presence of these hidden cracks, and we propose a model whereby moisture can penetrate the cracks in the busbar regions to initiate the reactions with the encapsulant to form acetic acid and attack the silver gridlines and their interface with the silicon. Reducing soldering induced damage could thus reduce these corrosion risks.

We also propose the use of UVF and front encapsulant layers with UV absorbing additives to enable easy imaging of the hidden cracks during product development. Such imaging can be a powerful tool to enable the optimization of materials, designs, equipment, and processes. We are especially concerned that modern high-speed soldering equipment has insufficient pre-heat and post-heat zones [2,4,5] to minimize soldering induced damage, and that the equipment vendors and panel manufacturers are "flying blind" without such imaging to see the hidden cracks.

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